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(54) REDUNDANCY CIRCUIT FOR SEMICONDUCTOR MEMORY DEVICE

(57) Abstract:

PURPOSE: To test a redundant cell without waiting the fusion of a fuse by placing the redundant circuit in exactly the same operation as that in normal use according to information on a defective cell detected by a tester in the midst of a wafer probe test.

CONSTITUTION: The circuit is constituted of the fuse 1 which is a nonelectric means and a storage means for information on the replacement of an abnormal cell and an n-channel FAMOS 5 which is an EPROM transistor(TR), and also has a latching means for storing their states and a control circuit 3 which writes their states selectively according to the address of the defective cell. Then the FAMOS TR 5 interposed between the fuse 1 and the ground is put in electric operation from outside to write the information for operating the redundant circuit. Consequently, a wafer probe can be tested without fusing the fuse in the state of the test.